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Comparative Study of CMOS Op-Amp In 45nm And 180 Nm Technology

Siddharth[1], Mehul Garg[2], Aditya Gahlaut[3]
Jaypee Institute of Information Technology, Noida, India

ABSTRACT
In this paper we have provided a method for designing a Two Stage CMOS Operational Amplifier which operates at 1.8V power supply using Cadence Virtuoso 45nm CMOS technology. Further, designing the two stage op-amp for the same power supply using Cadence Virtuoso 180nm CMOS Technology, keeping the slew rate of the op-amp same as that 45nm technology. The trade-off curves are computed between various characteristics such as Gain, Phase Margin,GBW,3db Gain etc. and the results obtained for 45n CMOS Technology is compared with those obtained for 180nm CMOS Technology It has been demonstrated that on lowering the technology and keeping the slew rate constant, the Power dissipation decreases..
Keywords - Op-Amp (Operational Amplifier), CMOS (Complementary Metal Oxide Semiconductor Field Effect Transistor), Slew Rate, Two-Stage, Cadence, 45nm, 180nm, Power Dissipation

I. INTRODUCTION

Operational Amplifiers are the basic building block of many analog circuits. They have wide applications in many analog circuit including switched capacitor filters, sigma delta A/D converter, sample and hold amplifiers etc.
The basic 2 stage operational amplifier consists of three sections [1] :

A.**Dual input Differential Amplifier:** In Fig. I, the transistors nm0, nm1, pm0 and pm1 form the first stage i.e. differential stage of the operational amplifier.nm0 and nm1 are nmos transistors whose gate acts as the differential input node. Gate of nmos nm0 is the inverting input and the gate of nmos nm1 is the non-inverting input. In this stage current is mirrored from nm0 by pm1 and pm0 and subtracted from the current through nm1.This current mirror topology is used for converting the differential input signal to single ended output signal.

B.**Bias String:** In Fig. I, the bias string block of the op-amp architecture is formed by transistor nm6 and nm7 that supplies a voltage between the gate and source of nm6 and nm4.nm6 and nm7 are diode connected and hence, it ensures that they operate in saturation region. The required biasing of the remaining transistors is controlled by their respective node voltages.

C.**Output Buffer:** The Output buffer, more commonly known as Second Gain Stage, comprises of transistor nm4 and pm4 in Fig. I. It is a common source amplifier which provides an additional gain to the amplifier. The output of the differential input stage acts as the input for this stage. The gain

provided by this stage is the product of transconductance of pm4 and the effective load resistance i.e. the output resistance of nm4 and pm4.
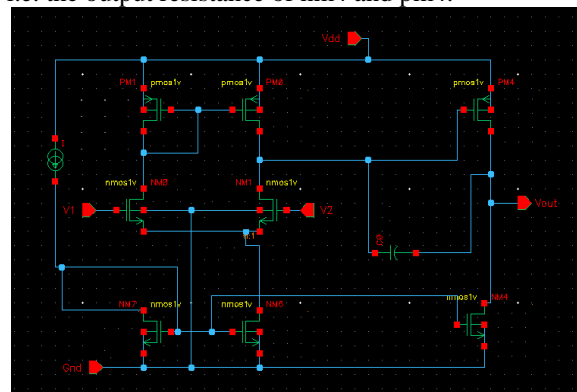

Figure I: circuit topology

II. DESIGN STRATEGY OF OP-AMP

The values of (w/l) for the transistors were calculated using the following basic equations[1] keeping the slew rate constant and equal to 1600V/µsec

$$Id=(\mu_n C_{ox}(w/l)Veff^2)/2 \qquad (1)$$
$$\text{transconductance,} g_m=\sqrt{(2\mu_n C_{ox}(w/l)I_d)} \qquad (2)$$
$$g_m=2I_d/C_c \qquad (3)$$
$$\text{Slew Rate,} SR=I_{bias}/C_c \qquad (4)$$
$$ICMR(+)=Vdd-\sqrt{(Id/\beta_{pm0})}-Vth_{pm0}(max.)+$$
$$Vth_{nm0}(min.) \qquad (5)$$
$$ICMR(-)=Vss-\sqrt{(Id/\beta_{nm0})}-Vth_{nm0}(max.)+$$
$$Vds_{nm6}(sat.) \qquad (6)$$
$$\text{Saturation Voltage,} V_{ds}=I_{ds}/\beta \qquad (7)$$

III. CHARACTERISTIC FEATURES OF OP-AMP

OPEN LOOP GAIN :

The ratio of change in output voltage to the change in voltage across the input terminals is known as open loop gain of the op-amp.It is also known as differential mode voltage amplification.[2]

COMMON MODE GAIN:

The ratio of output voltage to the input voltage when both the terminals of the op-amp are supplied same potential is known as common mode gain of op-amp.It is also known as common-mode voltage amplification.[2]

COMMON MODE REJECTION RATIO:

The ratio of differential voltage amplification to common-mode voltage amplification is known as common mode rejection ratio (CMRR). Ideally this ratio would be infinite with common mode voltages being totally rejected. [2]

SLEW RATE:

The rate at which the output changes with respect to the time required for a step change in the input is known as slew rate of the op-amp. It is generally expressed in the units of V/ μsec. [2]

INPUT COMMON MODE VOLTAGE RANGE:

The range of common-mode input voltage that may cause the operational amplifier to cease functioning properly if the input voltage goes beyond this range is known as input common mode voltage range.[2]

UNITY GAIN BANDWIDTH:

The range of frequencies within which the open-loop voltage amplification is greater that unity is referred as the unity gain bandwidth of the op-amp.[2]

TOTAL POWER DISSIPATION:

The total dc power supplied to the device less any power delivered from the device to a load is known as total power dissipation of the op-amp.[2]

At no load, $P_D = V_{DD} * I$ (8)

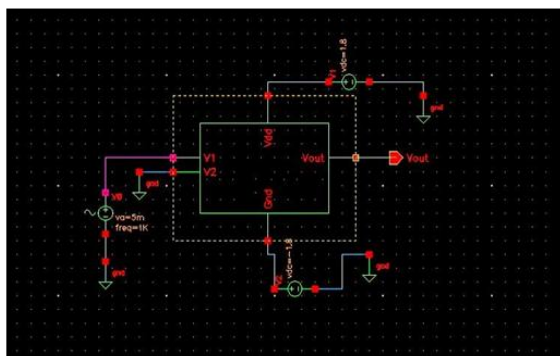# IV.   SIMULATION RESULTS
A. Test Circuit

Figure II: test circuit

B. Open Loop Gain:

Open Loop gain is the result of the AC Analysis carried out on the circuit with V_1(Inverting) connected with a sine wave having DC amplitude of 0V,AC amplitude of 1mV and frequency of 1   KHz and V_2(non-inverting) connected to ground.   Start Time =1Hz
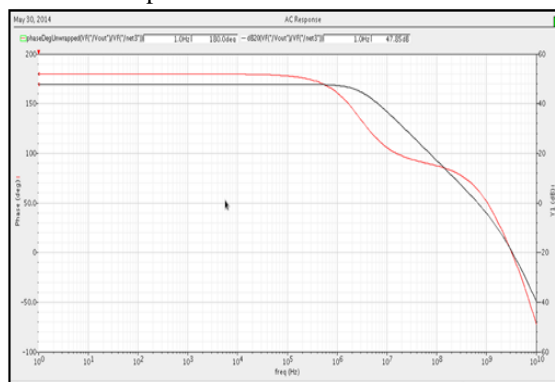
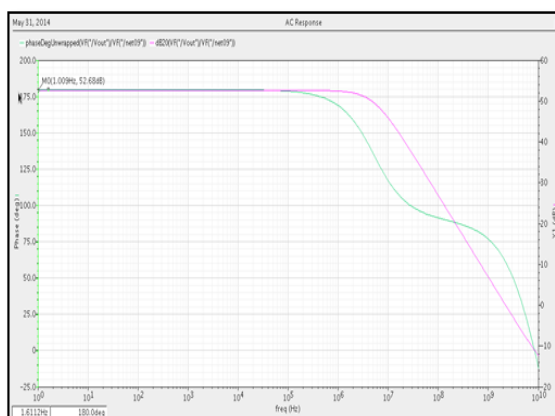Stop Time = 10 GHz

Figure III: open loop gain in 180 nm

Figure IV: open loop gain in 45nm
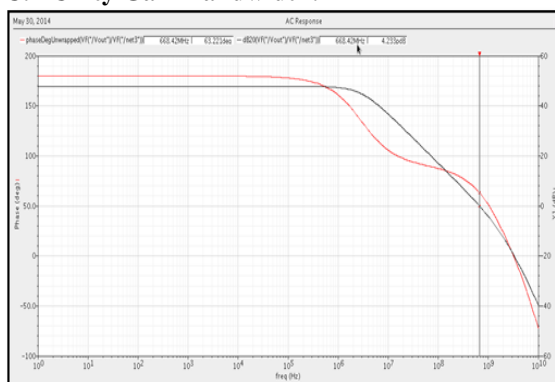
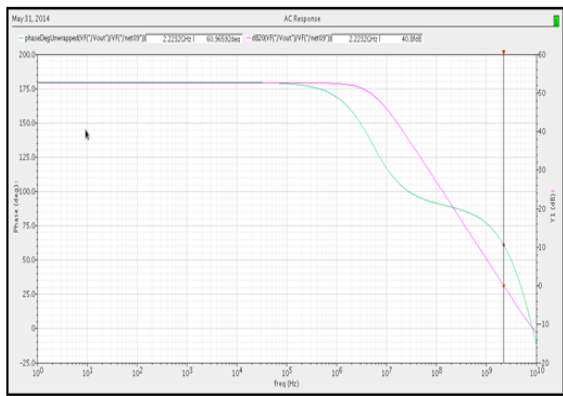## C. Unity Gain Bandwidth:
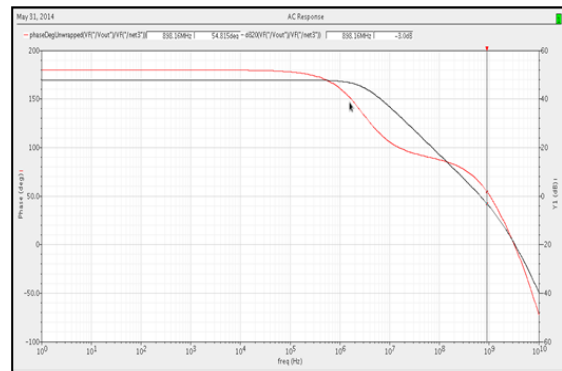

Figure V: unity gain bandwidth in 180nm

Figure VI: unity gain bandwidth in 45nm

D. Common Mode Gain:

For the calculation of common mode gain, both $V_{inverting}$ and $V_{non-inverting}$ terminals of the op-amp is connected to the common voltage source of sine wave having DC magnitude of 0V, AC amplitude of 1mV and frequency of 1KHz. AC analysis of the circuit is, then, carried out.
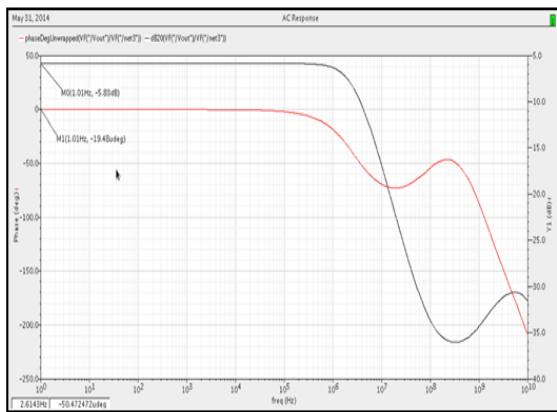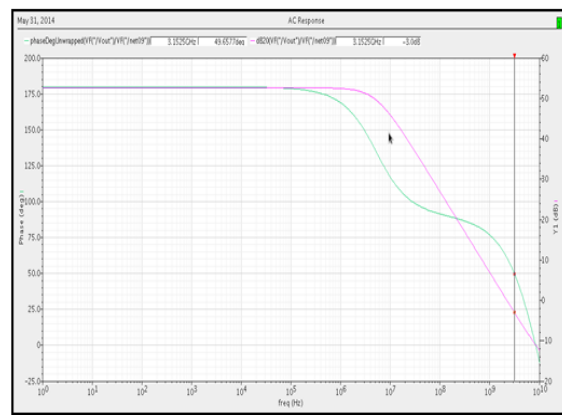

Figure VII: common mode gain in 180nm
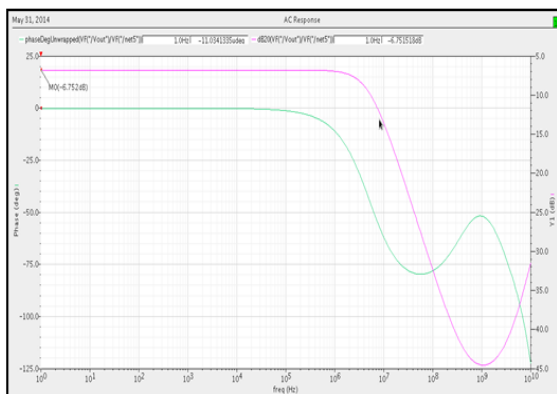

Figure VIII: common mode gain in 45nm

E. -3dB Gain Bandwidth

Figure IIIX: -3dB gain bandwidth in 180nm

Figure X: -3dB gain bandwidth in 45nm

V. RESULTS

The circuit in both technologies are simulated using

Power Supply: V_{dd} = 1.8V

V_{ss} = -1.8V

The results obtained after simulation of the circuit are tabulated below:

Table 1: Simulation Results

Results	180nm	45nm
Bias Current,I_{bias}	160uA	80uA
C_c	100fF	50fF
Open Loop Gain,A_d	47.85dB	52.68dB
Phase Margin,PM	63.221^o	60.9652^o
Unity Gain BW	668.42MHz	2.2232GHz
-3dB Gain BW	898.16MHz	3.1525GHz
Common Mode Gain, A_c	-5.83dB	-6.752dB
CMRR	53.68 dB	59.432 dB
ICMR(+)	1.6V	1.6V
ICMR(-)	0.8V	0.9V
Power Dissipation,P_d	3.5822mW	1.735mW

VI. CONCLUSION

As shown in the above results, taking the slew rate and the ICMR values constant, the power consumption of the two stage operational amplifier has decreased. It was also noticed that the gain at 45nm Technology was higher than that of 180nm technology circuit.

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